Specification and Simulation of Digital Systems – 15/16

Assignment Specification

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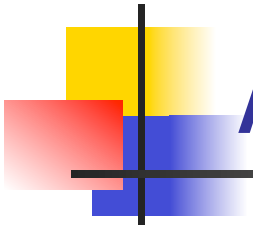
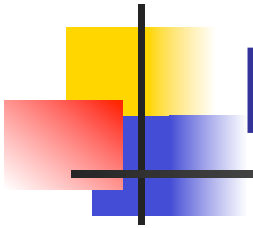


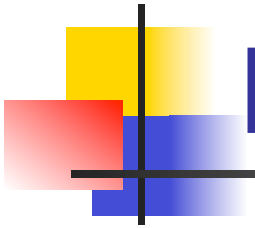
Assignment

- Individual project
- Design and Simulation of a System-on-a-Chip (SoC) including
  - Controller Unit
  - Data Memory
  - Xilinx IP peripheral
- Specific IP and simulation function for each student assignment



Description

- Design a self-test module able to perform a self-check of its operation at the power-up of the system
- The system will be hypothetically adopted on in-car infotainment
  - Once the car-power is turned on the system must execute a self-test to check if its operations are working properly.
  - The test must be performed within **500 μs**
  - In case of right operation the system must activate an **ok_status** signal

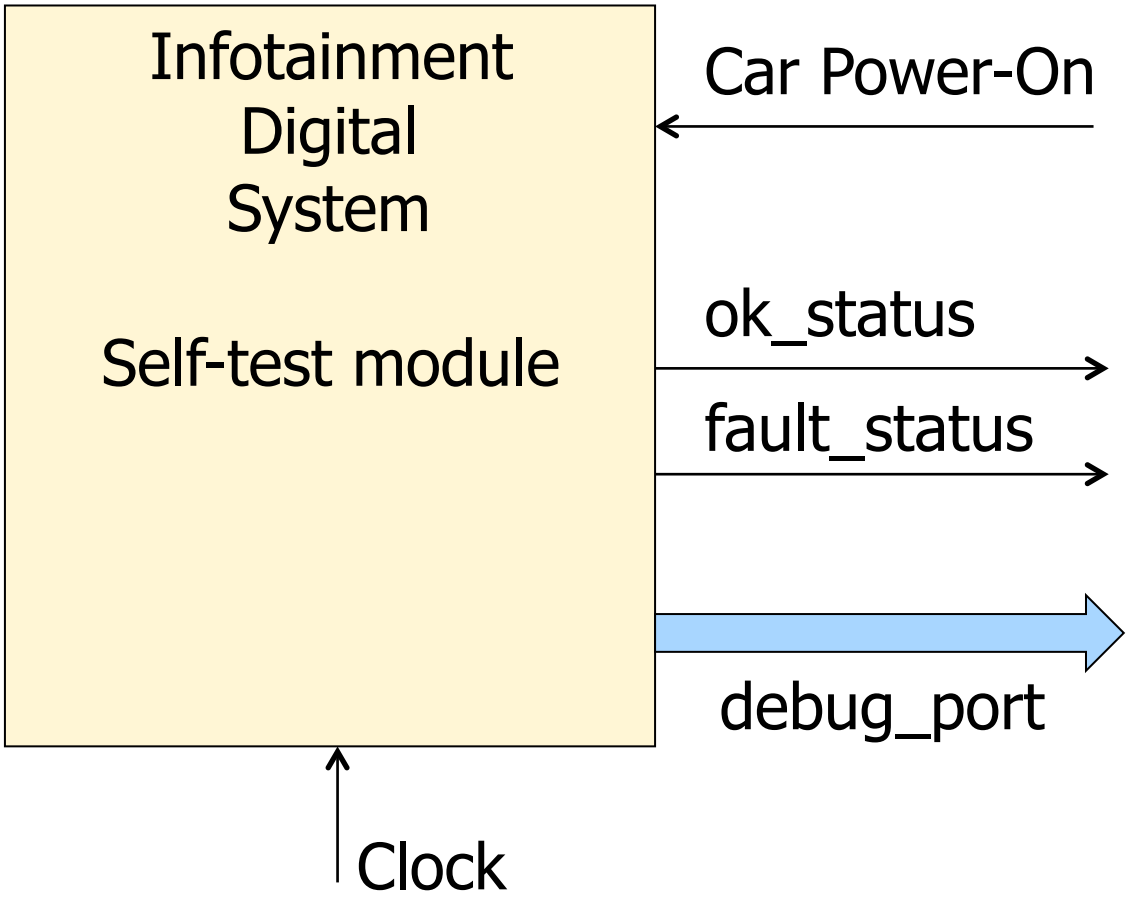


Description

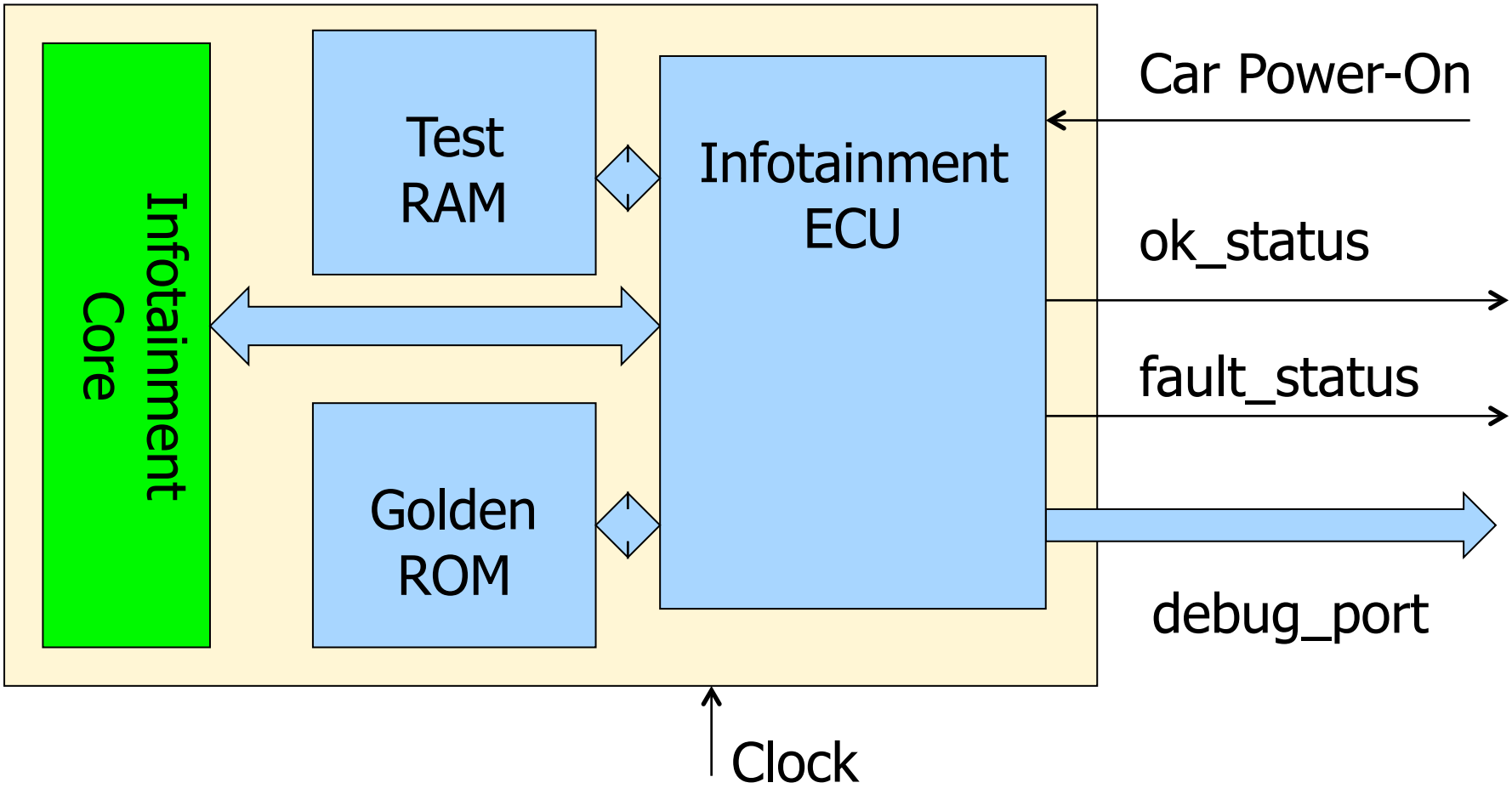
- If the system has a malfunction it must activate a **fault_status** signal and on a **debug-port** it provides the number of erroneous data followed by the erroneous results.

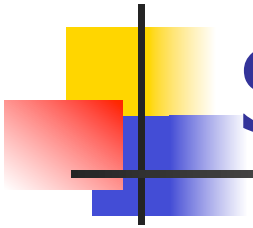
- The **width** of the debug-port must be correlated with the size of the test-pattern stimuli used.

Top-level entity



Internal architecture





Signals description

- The Infotainment system elaborates on the basis of a **150 MHz** clock signal.
- The car power-on signal is active for **2 μs**
- The ok_status signal remains active for **50 μs**
- The fault_status signal remains active until all the debug information are transmitted on the output:
  - Numbers of erroneous results: **1 μs**
  - Erroneous results: ***pattern dependent***

Internal component description

- Infotainment ECU: the main control unit of the entire infotainment digital system self-test module
- Test RAM: RAM memory block storing the results of the test
- Golden ROM: ROM memory block storing the input patterns and the expected "golden" (i.e., right) results
- Infotainment Core: **the Xilinx Logic Core unit selected by each student**