# Lorenzo Chelini

"In the end, we are our choices. Build yourself a great story."- Jeff Bezos

### Personal Data

BIRTH: Lucca, Italy | 23 December 1993 PHONE: +39 3347055531 EMAIL: l.chelini@icloud.com WEBSITE: http://lorenzochelini.azurewebsites.net/ LINKEDIN: /in/lorenzochelini GITHUB: chelini

# EDUCATION

07/2016-07/2017	MSc studies in COMPUTER ENGINEERING, Embedded System Track Chalmers University of Technology, Göteborg Exchange program with focus on dependable computing with empha- sis on system-level design of fault-tolerant systems, EDA-based design and verification methods, micro-system system packaging and modern micro- and nano-scale processing. MSc Thesis: "Power Estimation for DSP Components for Fiber-Optic Communication Systems" Advisor: Prof. Per Larsson-Edefors
SUMMER 2016	Summer school at EUROPEAN INNOVATION ACADEMY, Turin "From an Idea to a Tech Start-Up in 15 days" The European Innovation Academy (EIA) is a non-profit educational in- stitution recognized for excellence in tech entrepreneurship education. EIA educational programs are jointly developed with professionals of world class partner universities and companies: UC Berkeley, Stanford University, Google, Amadeus, IBM and Ferrero.
10/2015-07/2017	MSc studies in COMPUTER ENGINEERING, Embedded System Track <i>Polytechnic of Turin</i> , Turin Emphasis on: Computer Architecture, Real-time OS, Digital and Analog electronics, RTL and Logic level design for ASICs and FPGA, EDA and CAD-based synthesis and optimization of digital systems. Grade: 110/110
09/2012-09/2015	BSc in COMPUTER ENGINEERING University of Pisa, Pisa BSc Thesis: "RAPID Robotic Arm empowering People with Disabilities Project" Advisor: Prof. Enrico FANUCCI Grade: 101/110

# WORK EXPERIENCE

#### 2014-2016 | Junior ICT Officer

*Via Roma Agency s.r.l,* Lucca Implementation and management of the software applications and hardware infrastructure that support operations of the SME.

### PUBLIC PROJECTS

#### 2016 | **DLX**

Implementation of a five stages DLX pipeline processor. In this project I have refined the DLX processor from the RT level down to the physical layout. The project consists of four modules connected together according to the structural approach: a complex data path, an hardwired control unit, a data memory and an instruction memory. The code is written in VHDL.

#### 2015 | Self-Test Module

Design and simulation of a System-On-Chip including a Control Unit, Data Memory and a Xilinx IP peripheral. The code is written in VHDL.

#### 2015 | Proximity Alert System

System realized using HC-SR04 Ultrasonic Ranging Module, FRDM-K64F board and Micrium uC/OS. The code is written in C.

#### 2015 | **RAPID**

Robotic Arm Empowering people with Disabilities. The project has been presented at the ARTEMIS 2015 call brokerage event. The project consists of a robotic arm running a real-time software that is able to track objects selected by the user. The software is based on Intel Computer vision library OpenCV 3.0 and is written in C/C++.

#### 2014 | Force4

Well known game implemented using a p2p and client server architecture. Peer-to-peer relation established following client-server handshaking session. The code is written in C.

### LIST OF PUBLICATIONS

#### 2017 MSc Thesis: Power Estimation for DSP Components for Fiber-Optic Communication Systems

The thesis proposes and examines a power estimation method for Finite Impulse Response (FIR) filters used in short-reach fiber-optic communication systems, where limitations on size and power consumption start to become a critical design metric. ITALIAN:Mothertongue ENGLISH:Fluent SWEDISH:Basic Knowledge

# INTERESTS AND ACTIVITIES

I like spending time with friends and family. I love cooking and tasting new food. I try to travel as often as possible. I am an expert rower and active member of the local rowing club.

### References

References available upon request.